LISTING OF THE CLAIMS

1. (Original) A method for measuring integrated circuit processor power demand comprising:

calibrating one or more voltage controlled oscillators (VCOs) for use as ammeters;

calibrating a calibration current source, wherein the calibration current source draws current through an inherent resistance;

calculating the inherent resistance; and

calculating the processor power demand using a voltage that is measured across the inherent resistance.

2. (Original) The method of claim 1 wherein calibrating one or more VCOs further comprises:

providing a resistive ladder having a plurality of voltage taps;

applying voltages from selected ones of the voltage taps to each of the VCOs;

monitoring an output count from the VCO over a set period; and

storing, for each VCO, a table of output counts for each voltage.

3. (Original) The method of claim 2 wherein the plurality of voltage taps are known, evenly spaced voltages.

4. (Original) The method of claim 2 further comprising:

interleaving a VCO calibration cycle with other VCO measurements.

5. (Original) The method of claim 1 wherein calibrating a calibration current source further comprises:

providing a first variable current source and a second variable current source, wherein the second current source outputs more current than the first current source by a scaling factor;

identifying a target current level for the first current source, wherein the target current source is equal to a calibration current divided by the scaling factor;

applying an input to the first current source;

comparing an output current of the first current source to the target current level;

if the output current does not equal the target current level, adjusting the first current source input until the first current source output current is acceptable; and

storing the value of the first current source input that produces the acceptable output current.

6. (Original) The method of claim 5 wherein the calibration current is 16 Amperes.

7. (Original) The method of claim 5 wherein the input to the first current source is a four-bit signal, and wherein the bits are individually adjusted to change the first current source output current.

8. (Original) The method of claim 5 wherein the input to the first current source is a first four-bit signal and the input to the second current source is a second four-bit signal, and wherein when the same four-bit number is used for both the first and second current source inputs, the ratio of the second current source output current to the first current source output current is the scaling factor.

9. (Original) The method of claim 1 wherein calculating an inherent resistance further comprises:

stalling operations in cores of the processor;

measuring a first calibration voltage across the inherent resistance, while the second current source is off;

measuring a second calibration voltage across the inherent resistance, while the second current source is on and drawing a known current; and

calculating the inherent resistance using the difference between the first and second calibration voltage and the known voltage.

10. (Original) The method of claim 9 wherein a first calibration current through the inherent resistance is a current drawn by the stalled processor while the second current source is off; and

wherein a second calibration current through the inherent resistance is a current drawn by the stalled processor while the second current is on.

11. (Original) The method of claim 9 wherein the inherent resistance is a resistance in the power supply grid to the processor integrated circuit.

12. (Original) The method of claim 9 wherein the known current is 16 Amperes.

13. (Original) The method of claim 9 further comprising:

releasing the processor from a stalled state;

measuring the voltage across the inherent resistance while the processor is operating; and

calculating an operating power level for the processor.

14. (Original) The method of claim 1 further comprising:

repeating the calibration operations at periodic intervals to compensate for variations caused by temperature, operating voltage and/or age of the processor integrated circuit.

15. (Original) The method of claim 1 further comprising:

interleaving the calibration operations with measurement operations.

16. (Original) The method of claim 15 wherein a calibration cycle is completed within a thermal time constant of the processor integrated circuit.

17. (Original) A system for calibrating measurements in a processor integrated circuit die, comprising:

at least one voltage controlled oscillator (VCO);

a resistive ladder having a plurality of voltage taps, wherein the voltage taps are connectable to the VCO; and

a controller coupled to the output of the VCO, wherein the controller maintains a calibration table of VCO output counts for selected voltage inputs;

wherein the at least one VCO, the resistive ladder and the controller are constructed on the same die as the processor integrated circuit.

18. (Original) The system of claim 17 further comprising:

a first variable current source having a first input controlled by the controller; and

a second variable current source having a second input controlled by the controller;

wherein, when a same signal is applied to the first and second inputs, the output of the second current source is greater than the output of the first current source by a scaling factor.

19. (Original) The system of claim 18 wherein the first and second variable current sources are constructed on the same die as the processor integrated circuit.

20. (Original) The system of claim 18 further comprising:

a known resistance coupled to the first variable current source; and

an inherent resistance coupled to the second variable current source.

21. (Original) The system of claim 20 wherein the VCO is coupled across the inherent resistance, thereby allowing the controller to measure a voltage drop across the inherent resistance.

22. (Original) A computer program product comprising a computer usable medium having computer readable program code embedded therein, the computer readable program code comprising:

code for calibrating one or more voltage controlled oscillators for use as ammeters;

code for calibrating a calibration current source, wherein the calibration current source draws current through a inherent resistance;

code for calibrating the inherent resistance; and

code for calculating the processor integrated circuit power demand using a voltage that is measured across the inherent resistance.

23. (Original) The computer program product of claim 22 wherein the code for calibrating one or more VCOs further comprises:

code for applying voltages from selected voltage taps on a resistive ladder to each of the VCOs;

code for monitoring an output count from the VCO over a set period; and

code for storing, for each VCO, a table of output counts for each voltage.

24. (Original) The computer program product of claim 23 further comprising:

code for interleaving a VCO calibration cycle with other VCO measurements.

25. (Original) The computer program product of claim 22 wherein the code for calibrating a calibration current source further comprises:

code for providing a first variable current source and a second variable current source, wherein the second current source outputs more current than the first current source by a scaling factor;

code for identifying a target current level for the first current source, wherein the target current source is equal to a calibration current divided by the scaling factor;

code for applying an input to the first current source;

code for comparing an output current of the first current source to the target current level;

code for determining if the output current does not equal the target current level and for adjusting the first current source input until the first current source output current is acceptable; and

code for storing the value of the first current source input that produces the acceptable output current.

26. (Original) The computer program product of claim 25 wherein the input to the first current source is a first four-bit signal and the input to the second current source is a second four-bit signal, and wherein when the same four-bit number is used for both the first and second current source inputs, the ratio of the second current source output current to the first current source output current is the scaling factor.

27. (Original) The computer program product of claim 22 wherein the code for calibrating a inherent resistance further comprises:

code for stalling operations in cores of the processor;

code for measuring a first calibration voltage across the inherent resistance, while the second current source is off;

code for measuring a second calibration voltage across the inherent resistance, while the second current source is on and drawing a known current; and

code for calculating the inherent resistance using the difference between the first and second calibration voltage and the known voltage.

28. (Original) The computer program product of claim 27 wherein a first calibration current through the inherent resistance is a current drawn by the stalled processor while the second current source is off; and

wherein a second calibration current through the inherent resistance is a current drawn by the stalled processor plus the known current.

29. (Original) The computer program product of claim 22 further comprising:

code for releasing the processor from a stalled state;

code for measuring the voltage across the inherent resistance while the processor is operating; and

code for calculating an operating power level for the processor integrated circuit.

30. (Original) A system for measuring integrated circuit processor power demand comprising:

means for calibrating one or more voltage controlled oscillators (VCOs) for use as ammeters;

means for calibrating a calibration current source, wherein the calibration current source draws current through an inherent resistance;

means for calculating the inherent resistance; and

means for calculating the processor power demand using a voltage that is measured across the inherent resistance.

31. (Original) The system of claim 1 further comprising:

a resistive ladder having a plurality of voltage taps;

means for applying voltages from selected ones of the voltage taps to each of the VCOs;

means for monitoring an output count from the VCO over a set period; and

means for storing, for each VCO, a table of output counts for each voltage.

32. (Original) The system of claim 30 wherein the means for calibrating a calibration current source further comprises:

means for providing a first variable current source and a second variable current source, wherein the second current source outputs more current than the first current source by a scaling factor;

means for identifying a target current level for the first current source, wherein the target current source is equal to a calibration current divided by the scaling factor;

means for applying an input to the first current source;

means for comparing an output current of the first current source to the target current level;

means for adjusting the first current source input until the first current source output current is acceptable, if the output current does not equal the target current level; and

means for storing the value of the first current source input that produces the acceptable output current.

33. (Original) The system of claim 30 wherein the means for calculating an inherent resistance further comprises:

means for stalling operations in cores of the processor;

means for measuring a first calibration voltage across the inherent resistance, while the second current source is off;

means for measuring a second calibration voltage across the inherent resistance, while the second current source is on and drawing a known current; and

means for calculating the inherent resistance using the difference between the first and second calibration voltage and the known voltage.

34. (Original) The system of claim 33 further comprising:

means for releasing the processor from a stalled state;

means for measuring the voltage across the inherent resistance while the processor is operating; and

means for calculating an operating power level for the processor.